



PTO/SB/30 (08-00)

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RCE/2811

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**REQUEST
FOR
CONTINUED EXAMINATION (RCE)
TRANSMITTAL**

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.

See The American Inventors Protection Act of 1999 (AIPA).

Application Number	09/334,646
Filing Date	June 17, 1999
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2811
Examiner Name	S. Hu
Attorney Docket Number	0756-1984

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed. Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which established RCE practice.

1. Submission required under 37 C.F.R. § 1.114

a. Previously submitted

- Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
- Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- Other

b. Enclosed

- Amendment/Reply
- Affidavit(s)/Declaration(s)
- Information Disclosure Statement (IDS)
- Other

2. Miscellaneous

a. Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(l) required)

b. Other Petition for Extension of Time _____

c. Other Change of Correspondence Address Form _____

3. Fees The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. _____

i. <input type="checkbox"/> RCE fee required under 37 C.F.R. § 1.17(e)	12/04/2002 BABRAHA1 00000024 09334646
ii. <input type="checkbox"/> Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)	01 FC:1801 740.00 OP
iii. <input type="checkbox"/> Other _____	02 FC:1202 72.00 OP
b. <input checked="" type="checkbox"/> Check in the amount of \$1,174.00 enclosed	03 FC:1201 252.00 OP
c. <input type="checkbox"/> Payment by credit card (Form PTO-2038 enclosed)	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Eric J. Robinson	Registration No. (Attorney/Agent)	38,285
Signature		Date	November 26, 2002

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, Box RCE, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark Office on:

Name (Print/Type)	Ava M. Dixon	Date	November 26, 2002
Signature			

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of) Art Unit: 2811
Shunpei YAMAZAKI et al.) Examiner: S. Hu
Serial No. 09/334,646)
Filed: June 17, 1999)
For: SEMICONDUCTOR DEVICE AND)
FABRICATION METHOD)
THEREOF)

CERTIFICATE OF MAILING

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PRELIMINARY AMENDMENT

Honorable Commissioner of Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated July 26, 2002 please amend the above-
identified application as follows:

IN THE CLAIMS:

Please add new claims 104-121 as follows:

--104. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to
corresponding pixel electrodes among the plurality of pixel electrodes and respectively
supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit
for driving the plurality of first thin film transistors; wherein,

the plurality of second thin film transistors each has a plurality of channel
areas formed in a semiconductor layer subjected to laser annealing respectively, and